

REMARKS

Claim Rejections Under 35 USC §102

Claims 1, 3-5, 7-10, 12-15, 17-20 and 23-24 are rejected under 35 USC §102(e) as being anticipated by Xu, U.S. Patent No. 6,714,081.

Claims 1 and 15 are amended to recite that the reference cell includes first and second junctions coupled together to operate at different current densities. Support for these limitations may be found in the specification, e.g., at page 2, lines 33-34. The Examiner alleges that Xu teaches a reference cell that includes a pair of transistors (26). Applicant disagrees with this characterization. But even if transistors (26) if Xu are interpreted as a reference cell, it does not include any transistors that operate at different current densities. For at least this reason, claims 1 and 15 are not anticipated by Xu, nor are claims 3-5, 7-8 and 17-19 which depend from claims 1 and 15.

Claim 9 is amended to recite operating a bandgap cell to generate a PTAT current in a resistor. Claim 20 is amended to recite bias means for generating a bias signal by operating a bandgap cell to generate a PTAT current in a resistor. Support for these limitations may be found in the specification, e.g., at page 9, lines 6-7. Xu does not disclose a bandgap cell capable of generating a PTAT current in a resistor. For at least this reason, claims 9 and 20 are not anticipated by Xu, nor are claims 10, 12-14 and 24 which depend from claims 9 and 20.

Claims 1, 8, 9, 14, 15 and 20 are rejected under 35 USC §102(b) as being anticipated by Haefner, et al., U.S. Patent No. 5,699,014.

As discussed above, claims 1 and 15 recite that the reference cell includes first and second junctions coupled together to operate at different current densities. Claim 9 recites operating a bandgap cell to generate a PTAT current in a resistor. And claim 20 recites bias means for generating a bias signal by operating a bandgap cell to generate a PTAT current in a resistor. The Examiner alleges that Haefner teaches a reference cell that includes a pair of transistors (720 and 725). Applicant disagrees with this characterization, but even if transistors 720 and 725 are interpreted as a reference cell, it does not include any transistors that operate at different current densities, and it does not generate a PTAT current in a resistor. For at least these reasons, claims 1, 8, 9, 14, 15 and 20 are not anticipated by Haefner.

Claims 1, 8, 9, 14, 15 and 20 are rejected under 35 USC §102(b) as being anticipated by Monticelli, U.S. Patent No. 4,618,816.

Claims 1 and 15 are amended to recite that the first component is coupled to a summing node between a first resistor coupled and a first junction. Support for this limitation can be found in the specification, e.g., nodes N42 in Figs. 7, 8 and 9. Monticelli discloses a resistor 20 coupled to a junction (4x) of transistor 13, but no other components are coupled to that node. For at least this reason, claims 1 and 15 are not anticipated by Monticelli, nor is claim 8 which depends from claim 1.

Claim 9 is amended to recite generating a PTAT current in a first resistor, and coupling a compensation current to the first resistor, thereby summing the PTAT current and the compensation current. Claim 20 is amended to recite that the compensation current is coupled to the first resistor, thereby summing the PTAT current and the compensation current. Support for these limitations can be found in the specification, e.g., page 9, lines 6-7. Monticelli discloses generating a PTAT current in a resistor 20 (col. 3, lines 21-22; col. 4, line 28), but Monticelli does not disclose summing a compensation current with the PTAT current. For at least this reason, claim 9 is not anticipated by Monticelli, nor is claim 14 which depends from claim 9.


Conclusion

Applicant requests reconsideration in view of the foregoing amendments and remarks. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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